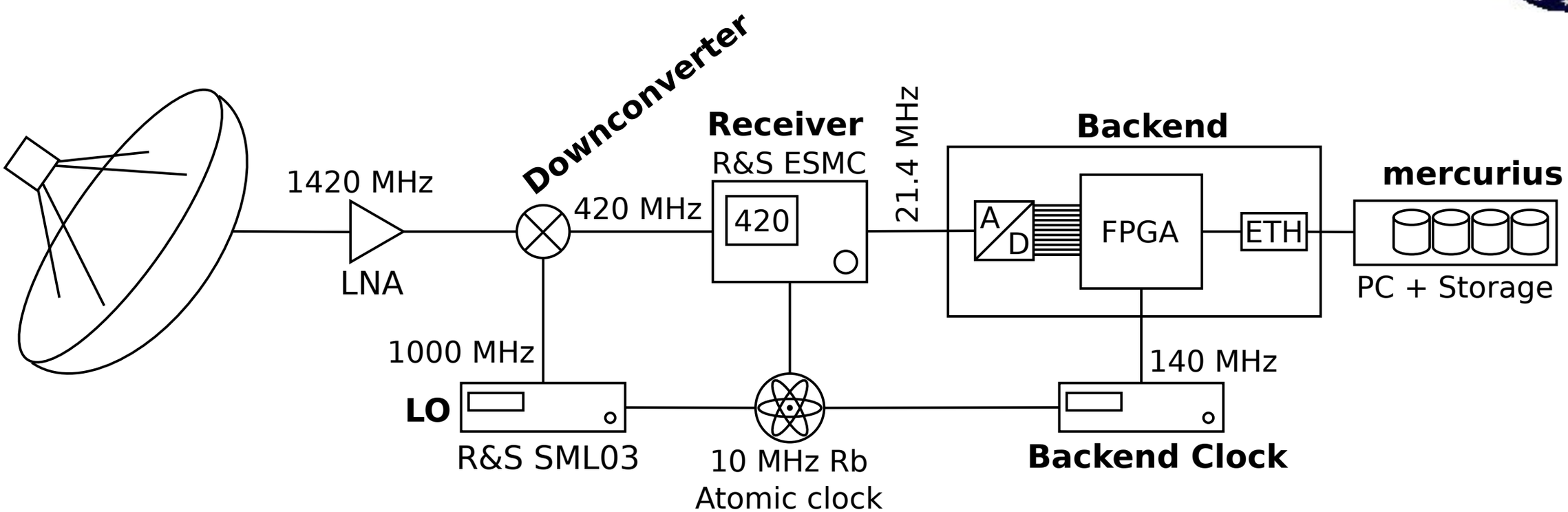
FPGAs bij CAMRAS

Paul Boven
PE1NUT

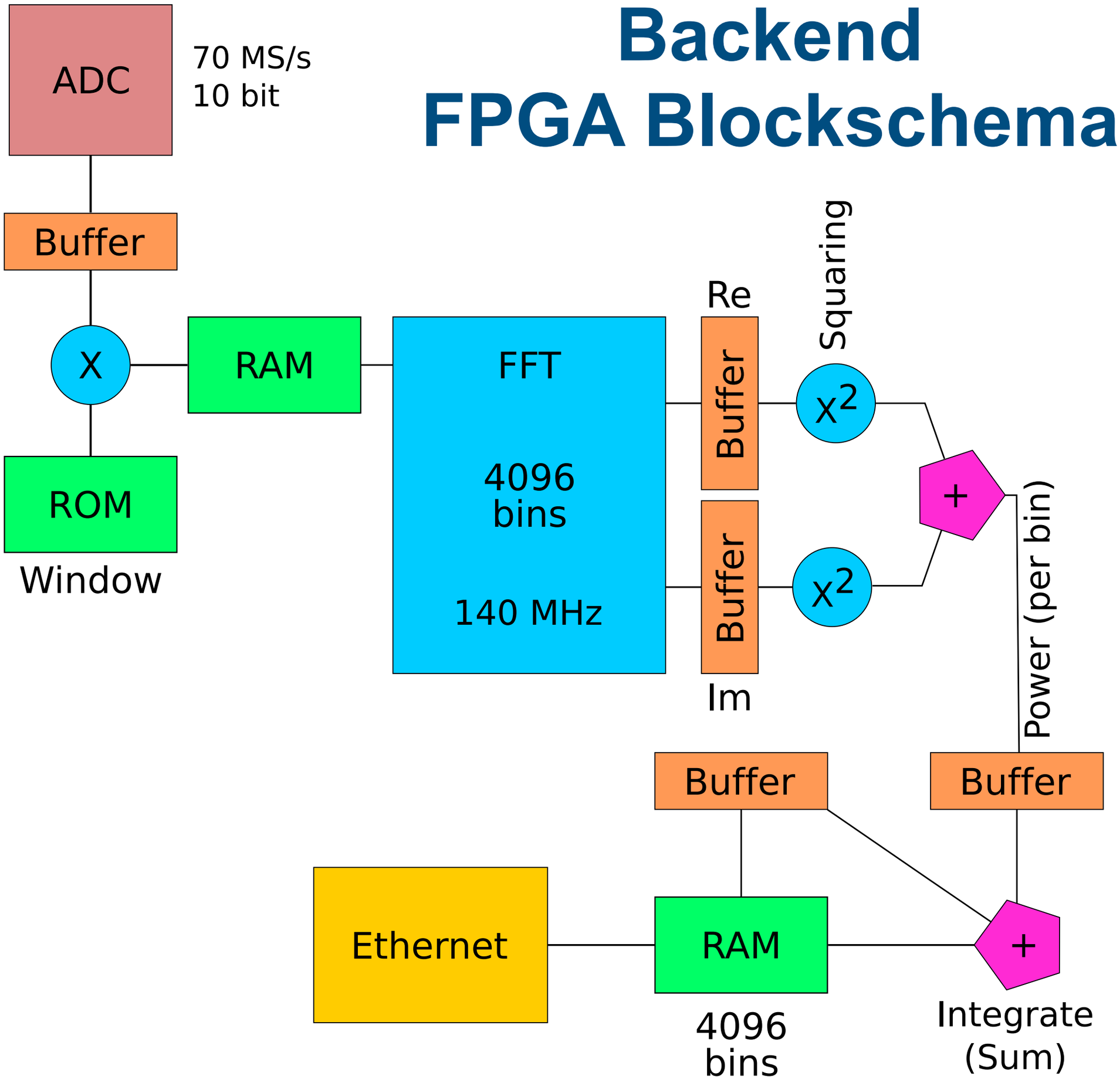
RF Seminar 2019-06-15 Dwingeloo

Signaal Schema DT

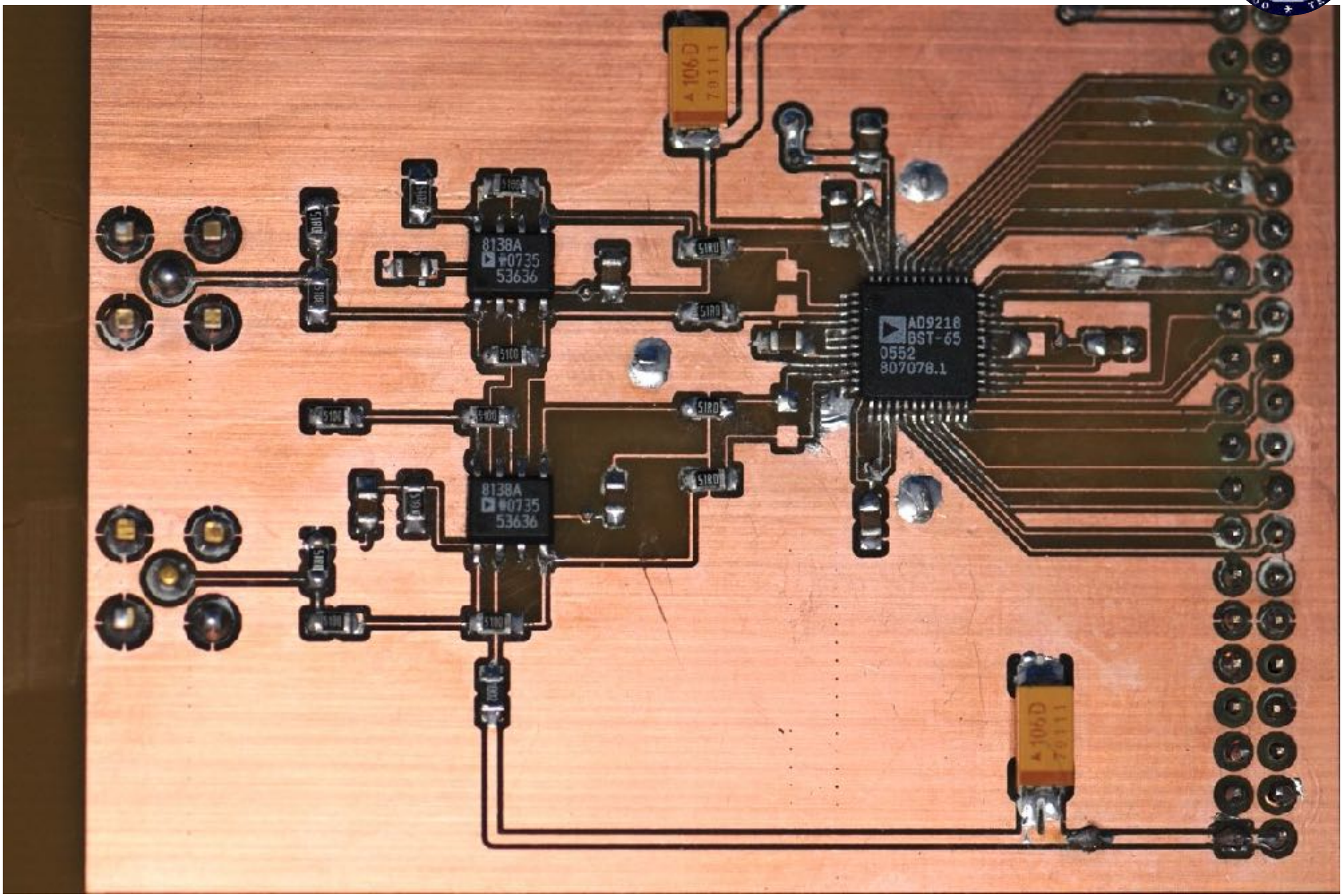


- Hoornantenne en LNA in het brandpunt
- Downconversie naar 21.4 MHz (via 420 MHz)
- IF Bandbreedte: ~25 MHz, gecentreerd 21.4 MHz
- Backend: Sampling op 70 MS/s
- Alle LOs gelockt aan ‘huisstandaard’

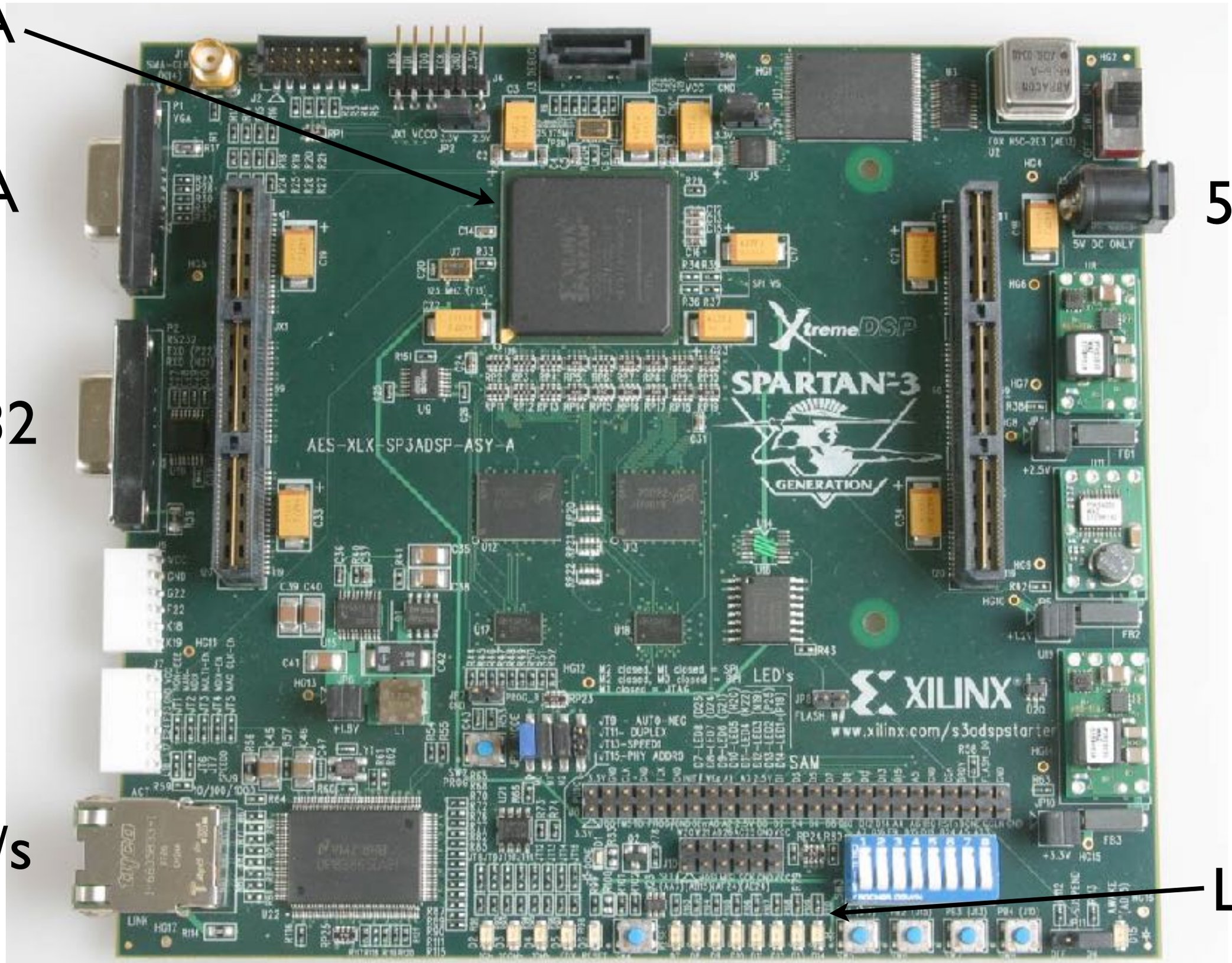
Backend
FPGA Blockschema



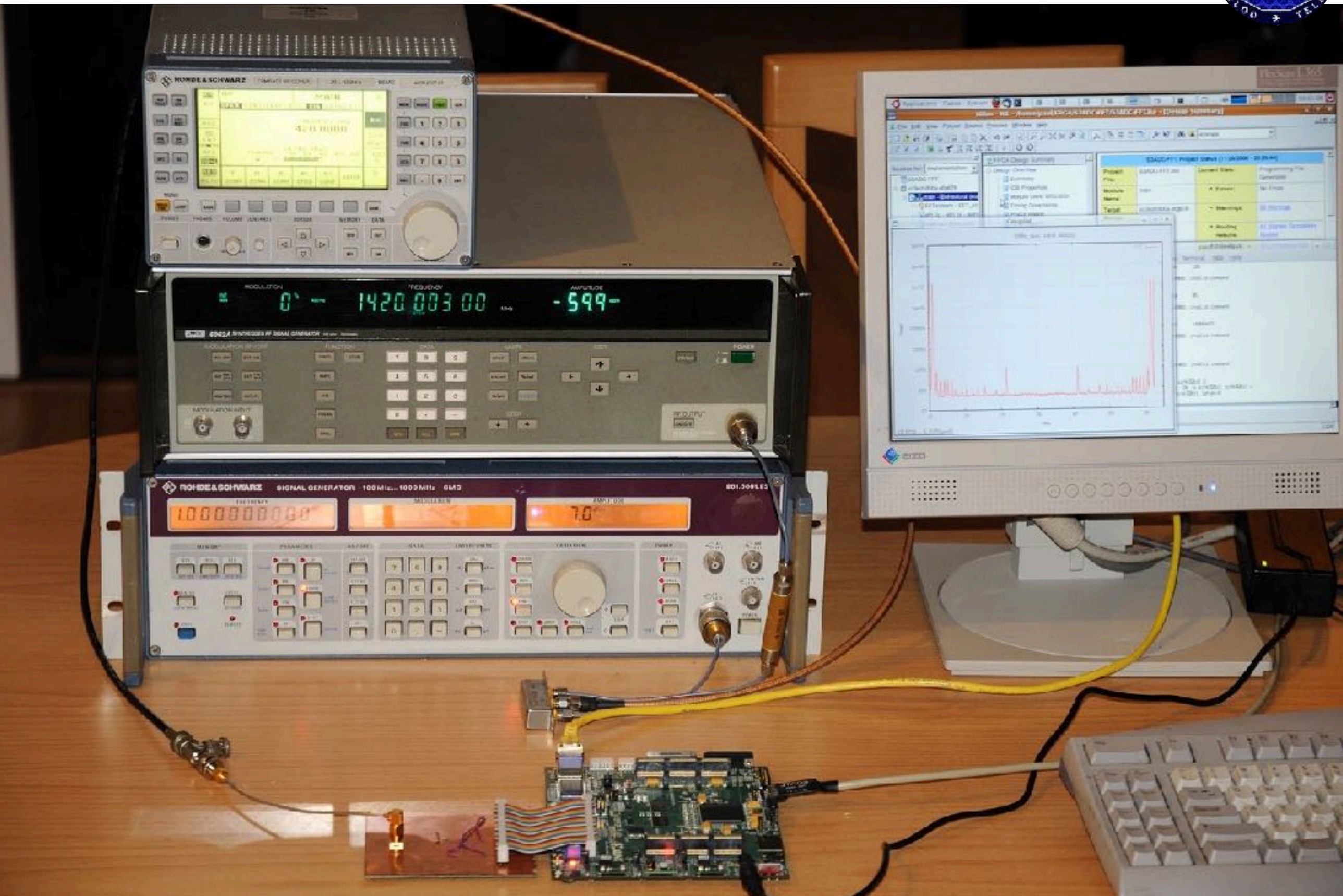
AD9218 65MHz dual 10bit A/D converter



Xilinx Spartan-3A DSP starter kit



Op mijn keuken tafel (2008)



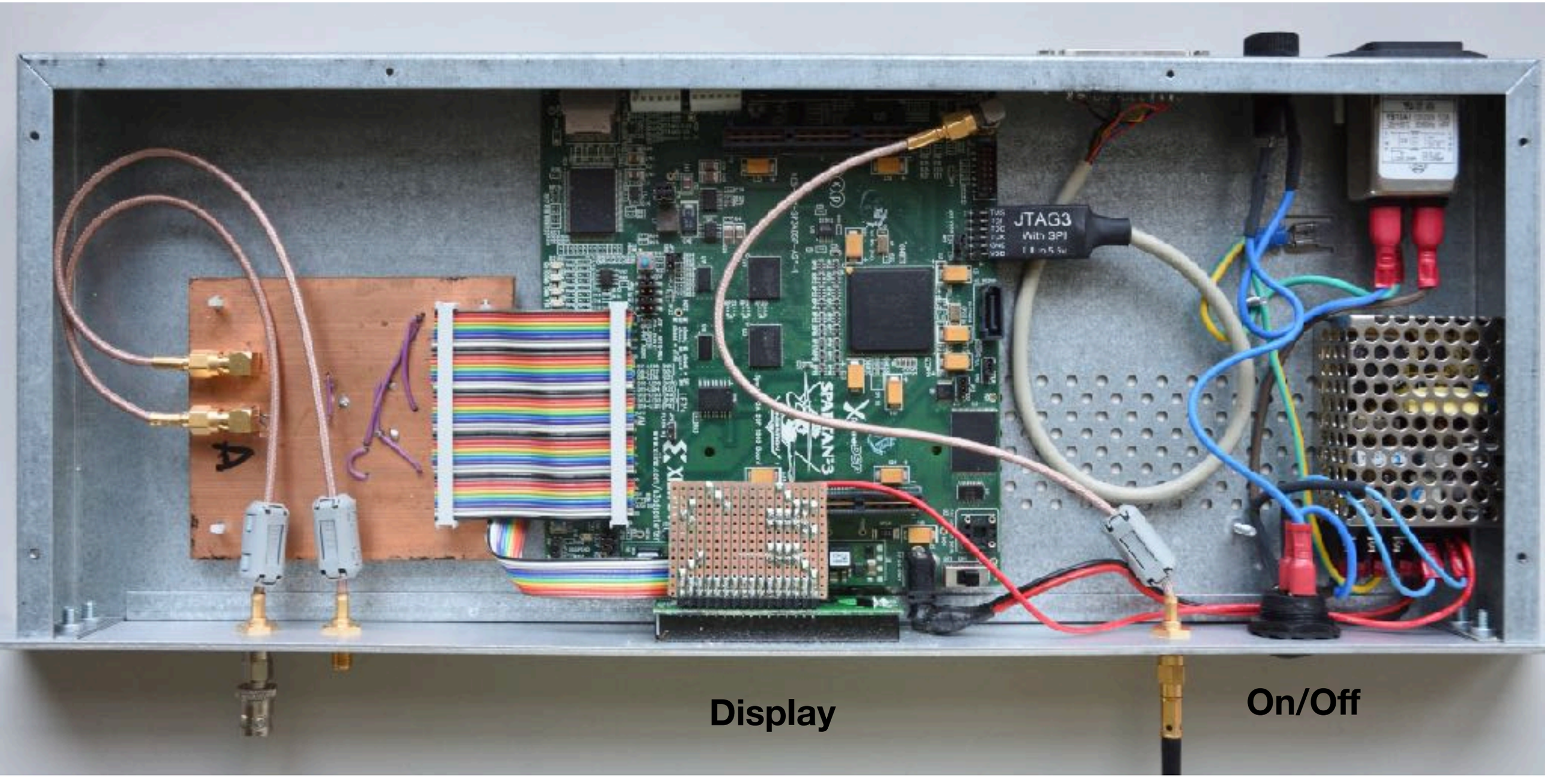
Ingebouwd (2010)

Ethernet

JTAG (Parallel)

Fuse

Mains



Inputs

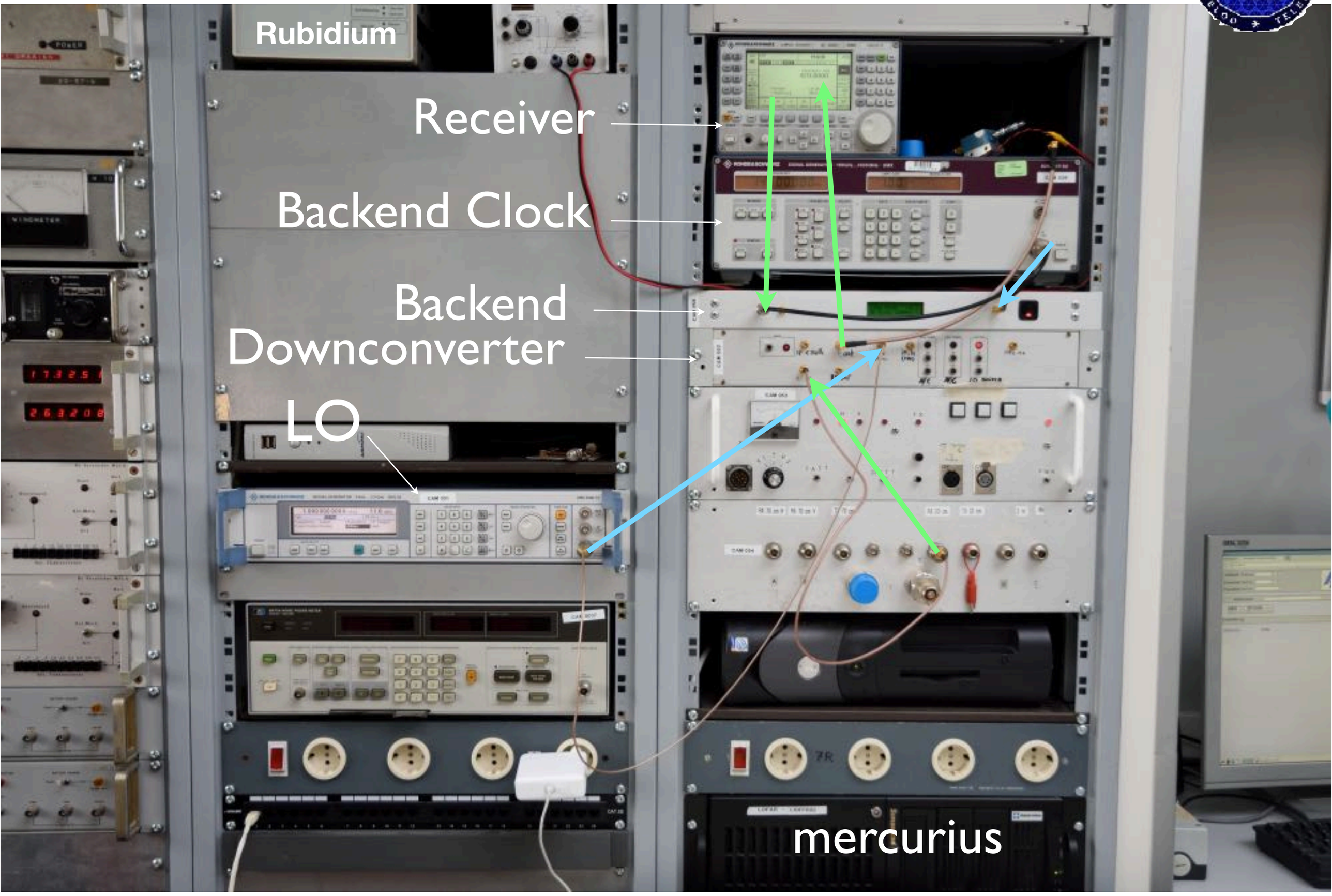
Display

On/Off

Clock

CAMRAS Back End

Signaal Keten (in de DT)



Backend Firmware

Pulsar mode

- 512 samples, 256 bins, 64 integrations
- 137 kHz resolution
- 2136 spectra per second

Line mode

- 4096 samples, 2048 bins, 64 integrations
- 17.1 kHz resolution
- 267 spectra per second

Raw mode (ADC mode)

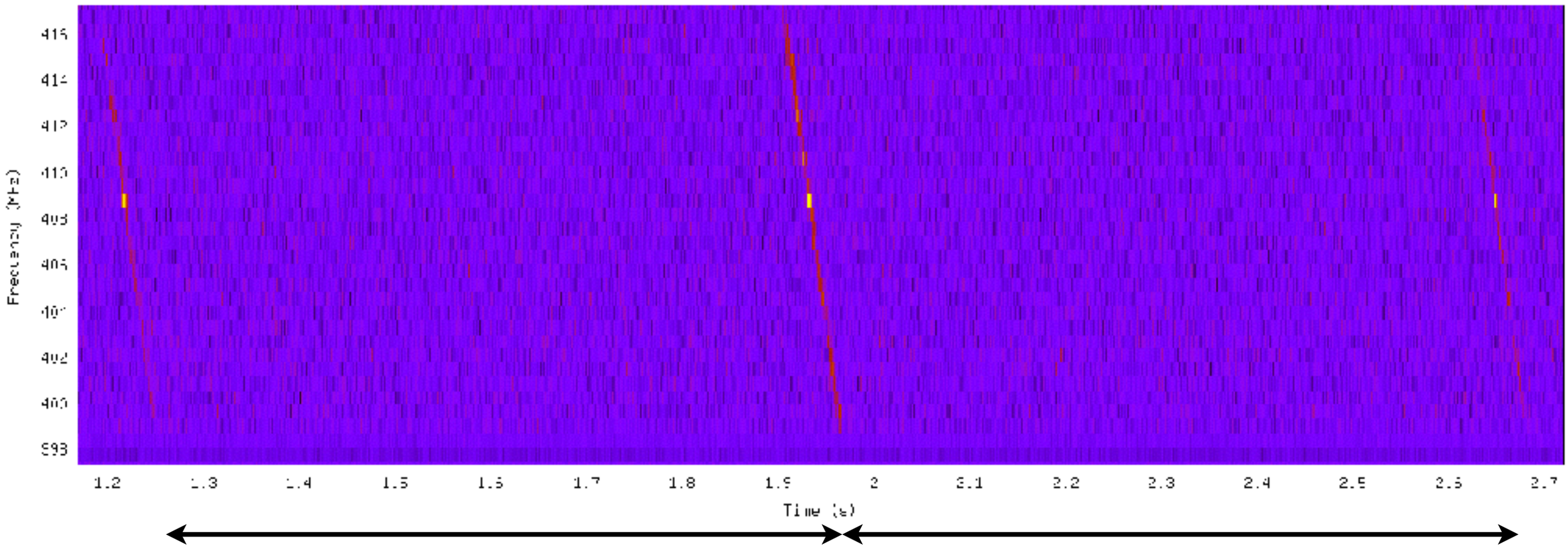
- 70M samples / second, 10 bit
- Sends 700Mb/s to RAID server
- 300GB per hour

Draaiende lijn geeft timing van backend aan

SDR mode (GNU Radio Compatible)

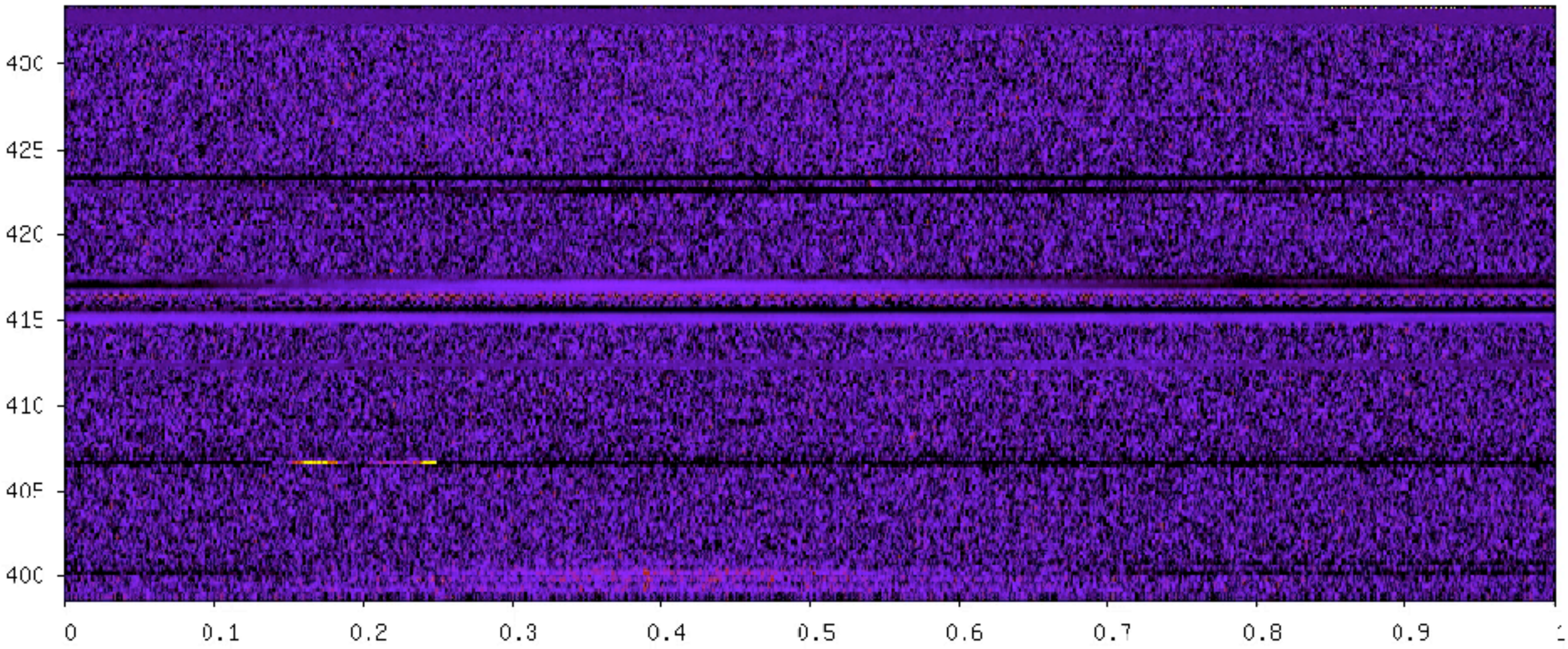
- Output: 5 MS/s IQ (5MHz)
- 16 bit interleaved

Pulsar Signaal

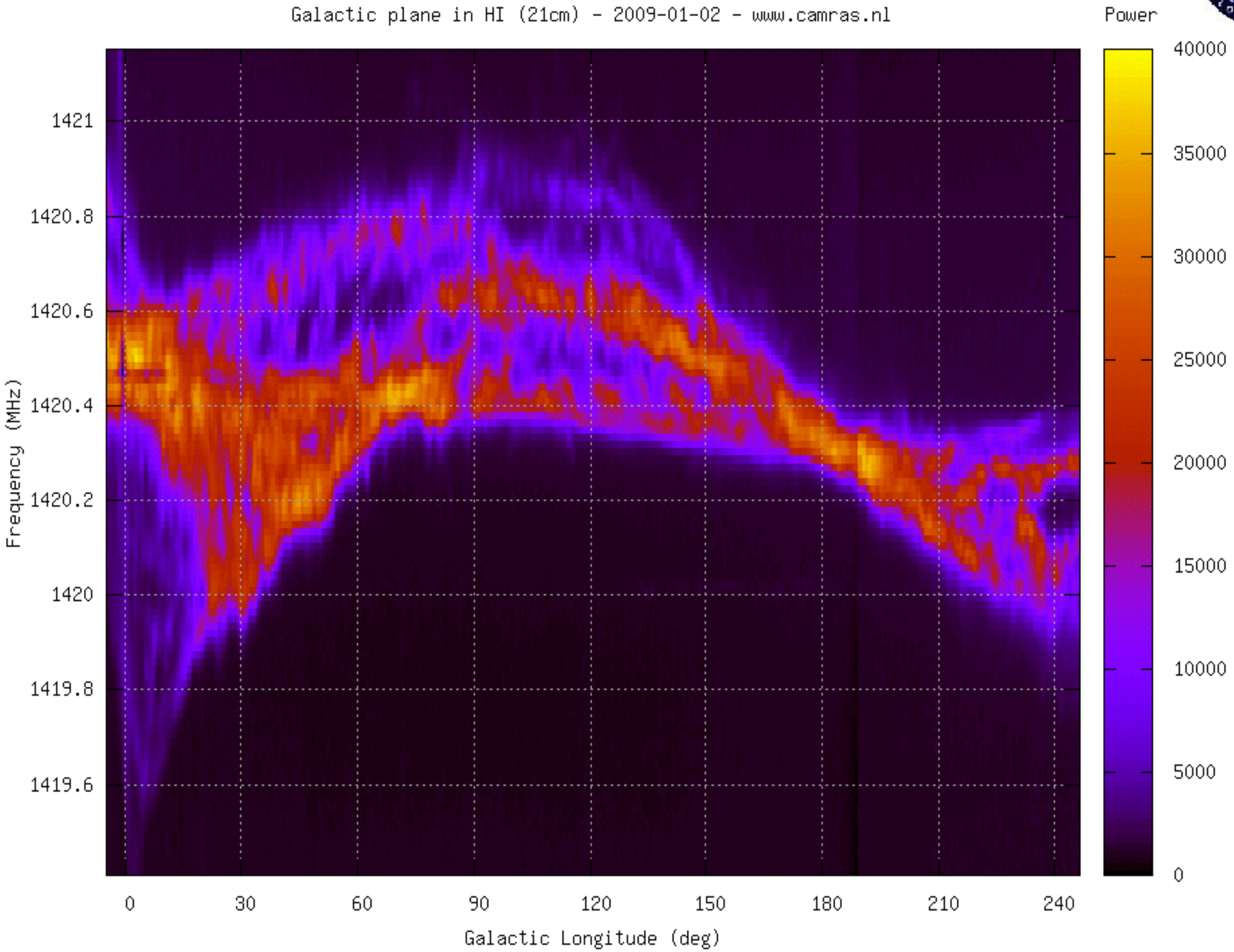


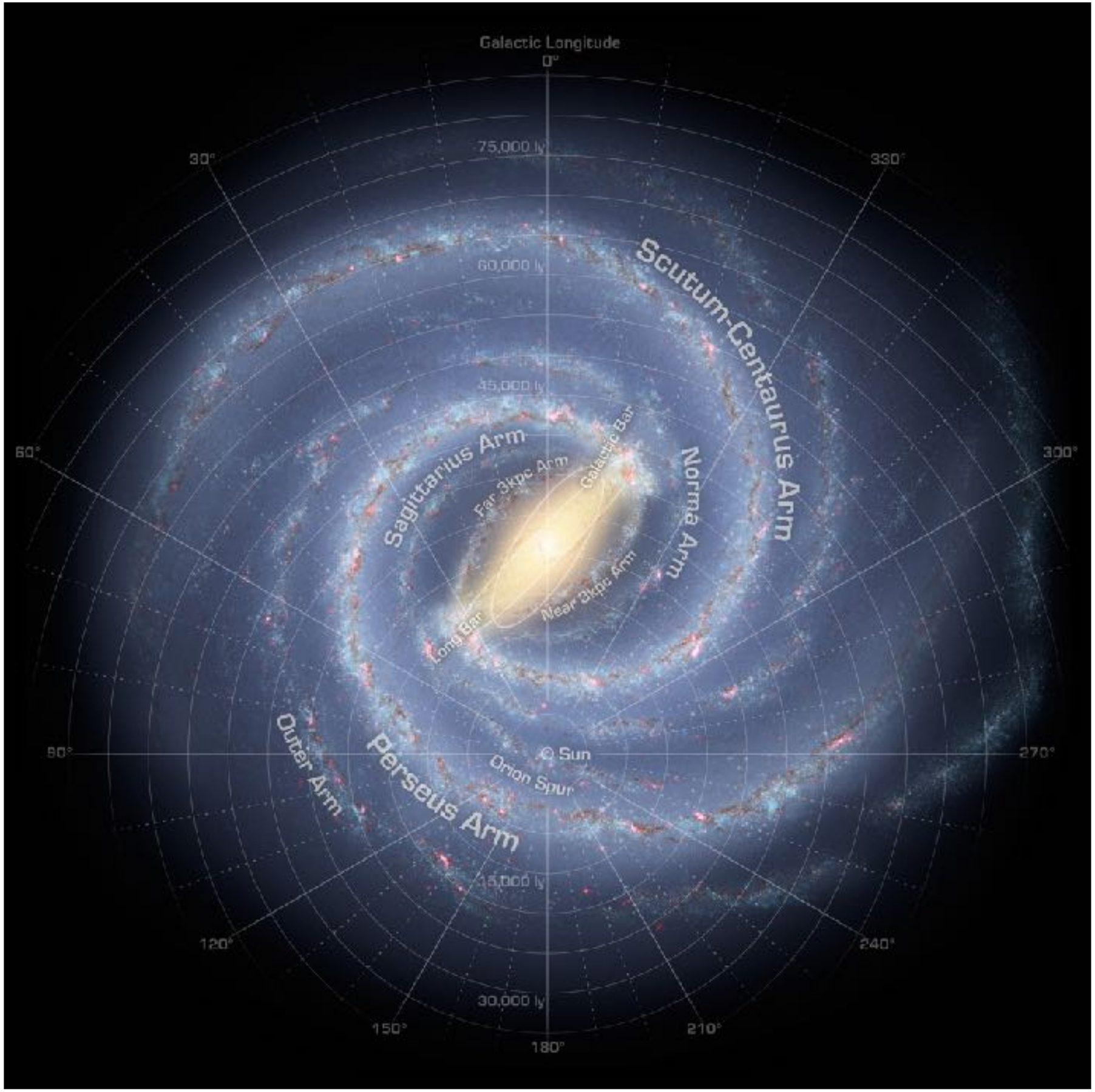
Vaste afstand tussen de pulsen, periode is heel stabiel.
Pulsen staan scheef door ‘dispersie’

Pulsar B0329+54



Waterstof in onze Melkweg

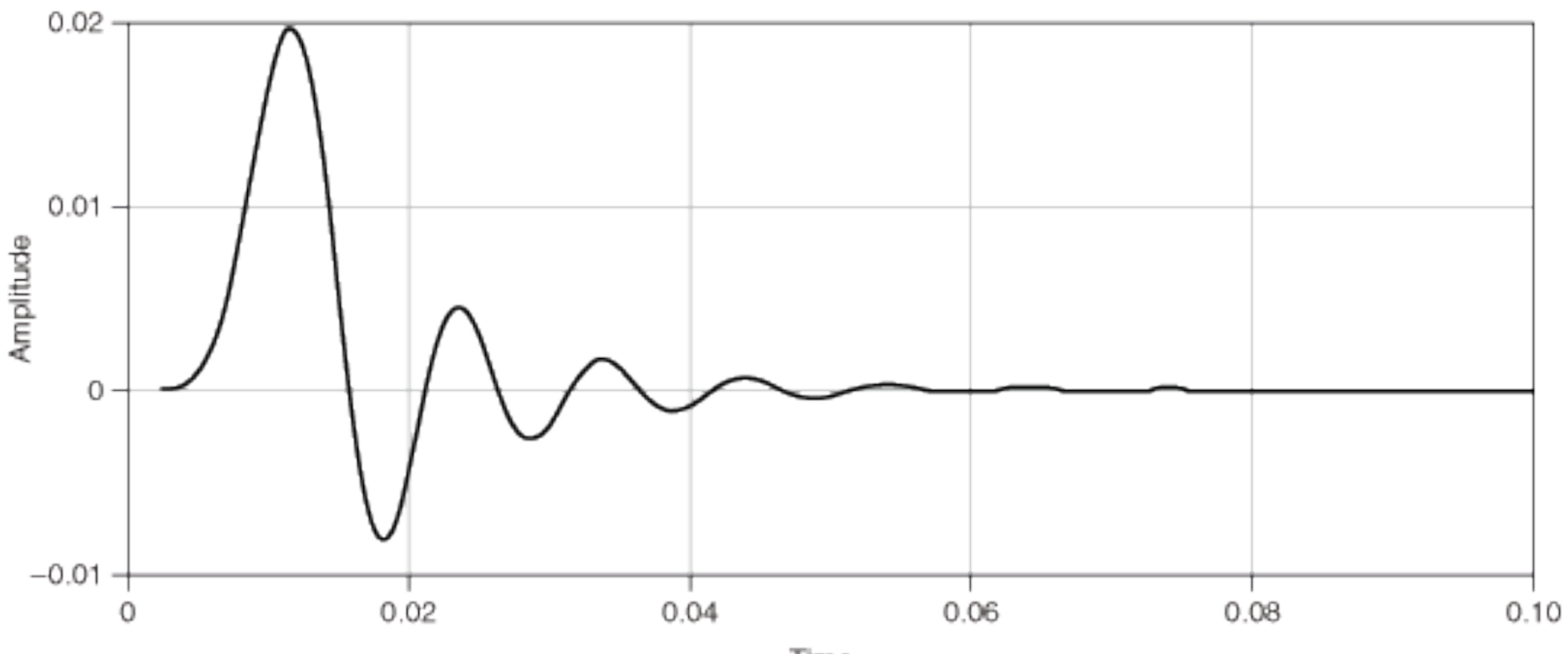



Galactic Longitude
0°
30°
330°
60°
300°
90°
270°
120°
240°
150°
210°
180°
75,000 ly
60,000 ly
45,000 ly
30,000 ly
15,000 ly
Scutum-Centaurus Arm
Norma Arm
Sagittarius Arm
Far 3kpc Arm
Galactic Bar
Near 3kpc Arm
Long Bar
Perseus Arm
Outer Arm
Sun
Orion Spur

Finite Impulse Response

Er zijn veel manieren om een filter te begrijpen

- Tijd domein - wat gebeurt er met de samples?
- Frequentie domein - wat gebeurt er bij welke frequentie?
- Impuls respons - Hoe ziet de output er uit van 1 puls?



Finite Impulse Response

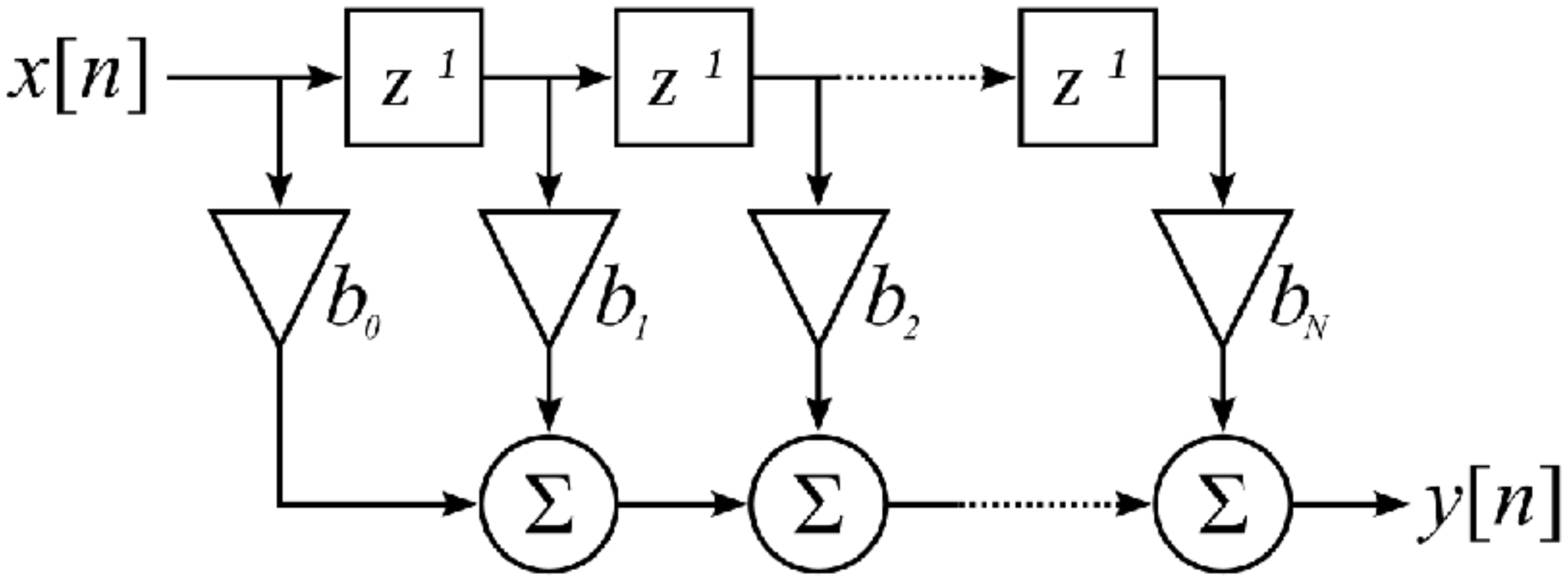


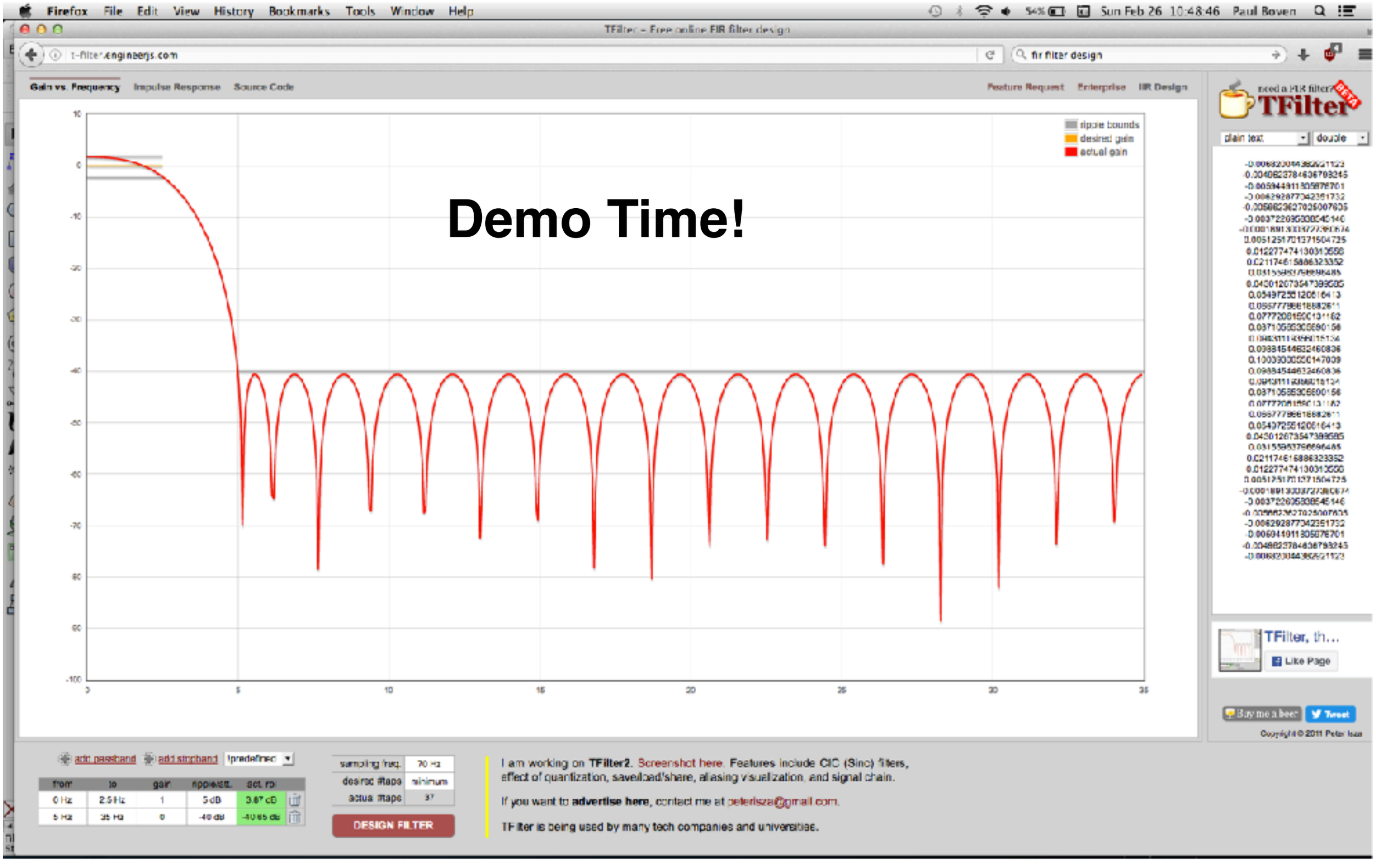
Image Source: Wikipedia

- x[n]: Input samples
- z^{-1}: Vertraging (delay van 1 sample)
- b_n: Coefficienten
- Σ: Optellen
- y[n]: Gefilterde samples

Finite Impulse Response

- Coefficienten bepalen gedrag van het filter
  - Low-pass, Band-pass, High-pass, phase shifter, …
- Scherper, vlakker, dieper -> Meer coëfficiënten
- Meer coefficients -> meer vertraging, meer rekenwerk
- Hoe komen we aan die coëfficiënten?
  - In GnuRadio: firdes.low_pass_2(gain, sample rate, cutoff frequency, transition width, attenuation)
  - Online: http://t-filter.engineerjs.com/

T-Filter


Firefox File Edit View History Bookmarks Tools Window Help
Sun Feb 26 10:48:46 Paul Boven
TFilter – Free online FIR filter design
t-filter.engineerjs.com
fir filter design
Gain vs. Frequency
Impulse Response
Source Code
Feature Request
Enterprise
IIR Design
ripple bounds
desired gain
actual gain
Demo Time!
need a FIR filter?
TFilter
BETA
plain text
double
add passband
add stopband
predefined
from
to
gain
ripple/att.
act. ripple
0 Hz
2.5 Hz
1
5 dB
3.87 dB
5 Hz
35 Hz
0
-40 dB
-40.65 dB
sampling freq.
70 Hz
desired #taps
minimum
actual #taps
37
DESIGN FILTER
I am working on TFilter2. Screenshot here. Features include CIC (Sinc) filters, effect of quantization, save/load/share, aliasing visualization, and signal chain.
If you want to advertise here, contact me at peterisza@gmail.com.
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Finite Impulse Response

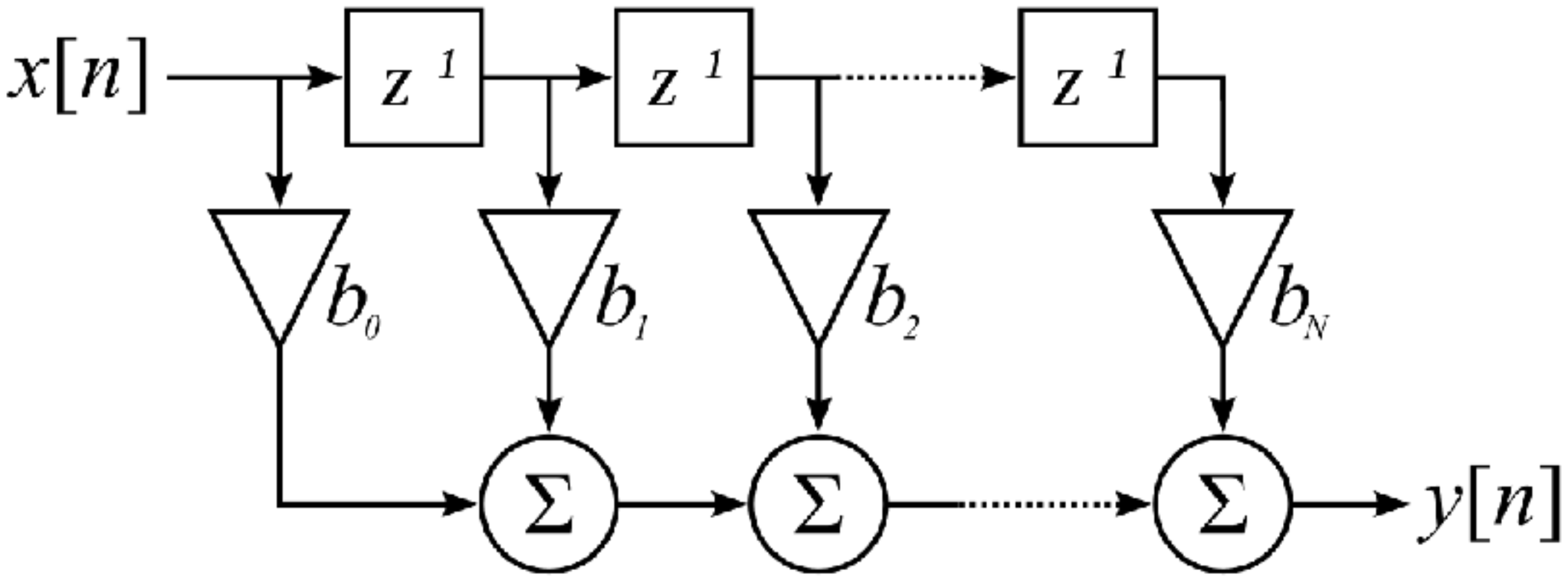

Image Source: Wikipedia

- x[n]: Input samples
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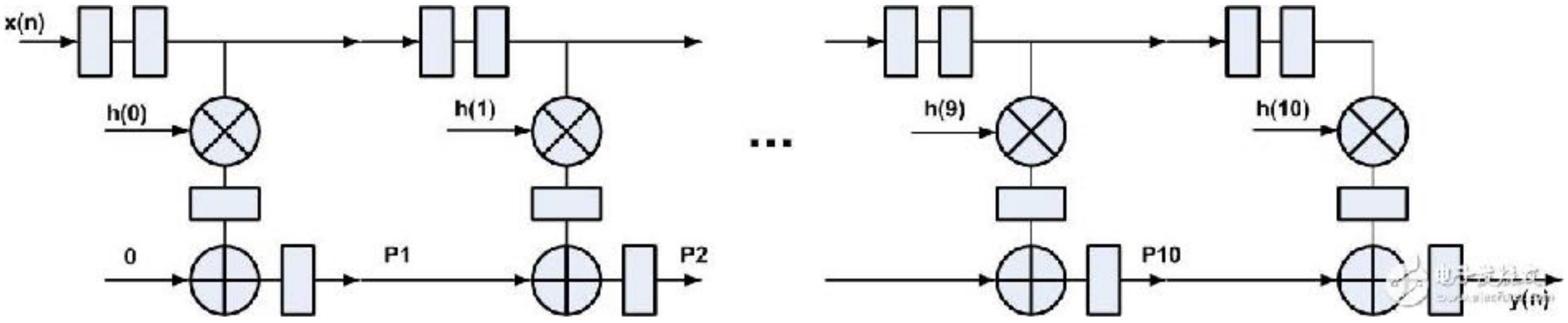
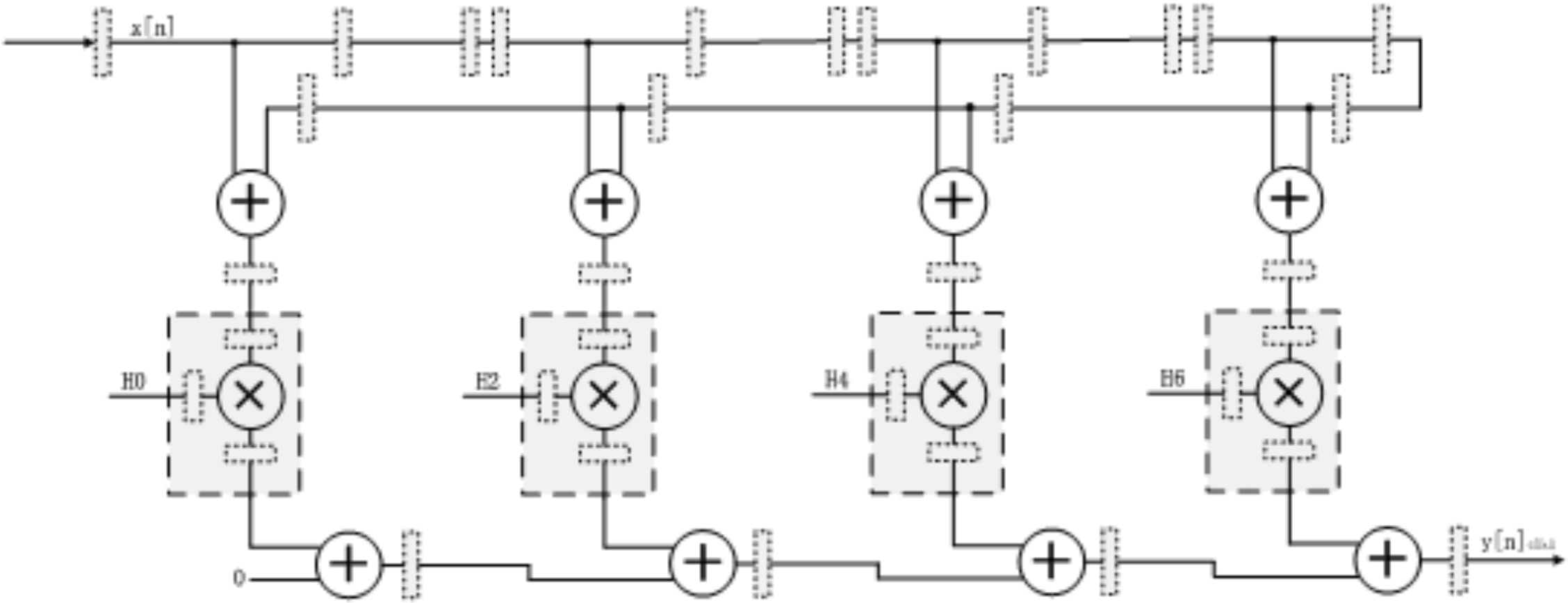
- b_n: Coefficienten
- Σ: Optellen
- y[n]: Gefilterde samples

FIR in FPGA: Systolic



- Voeg extra delays toe in input en output chain (pipeline)
- Optelling neemt nu maar 2 inputs, kan met kloksnelheid
- Delay van het filter neemt toe

Systolic Symmetric Half Band

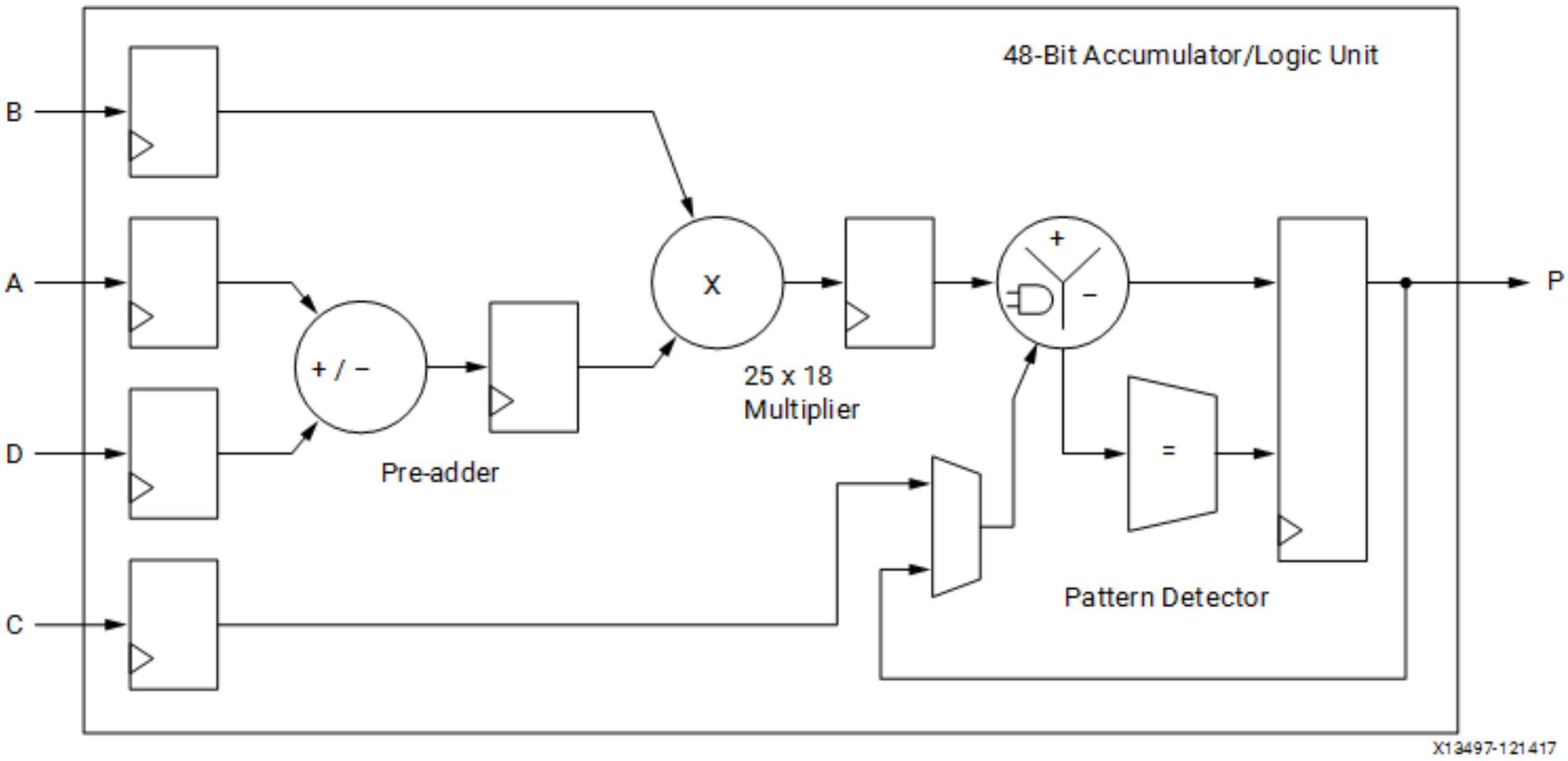


Maakt gebruik van:

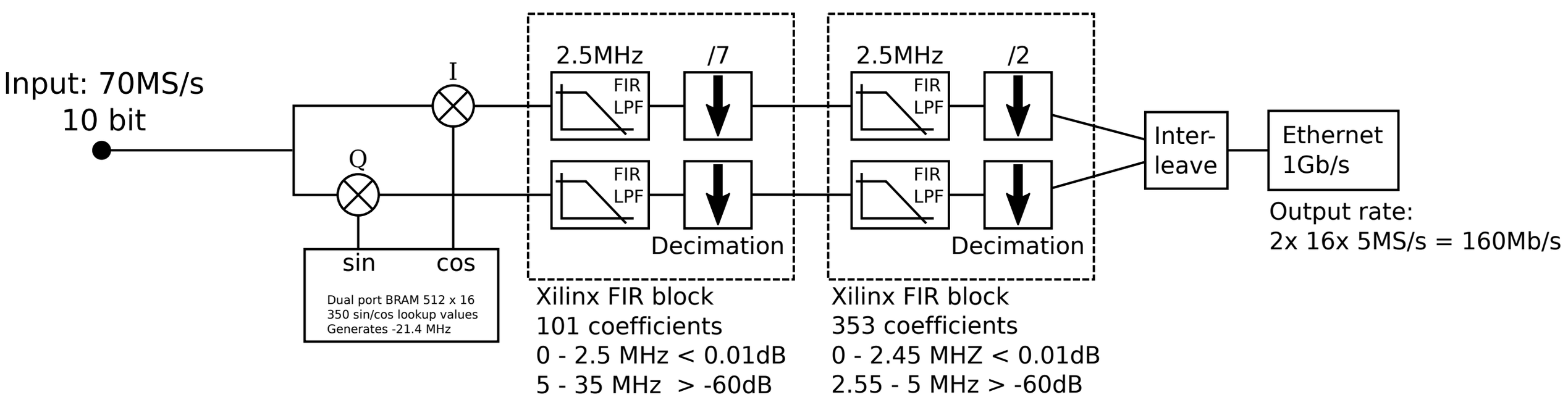
- Helft van de coëfficiënten is nul
- Coëfficiënten zijn symmetrisch
- Gebruikt maar 1/4e van de multipliers

Past perfect in de hardware DSP blocks van de FPGA

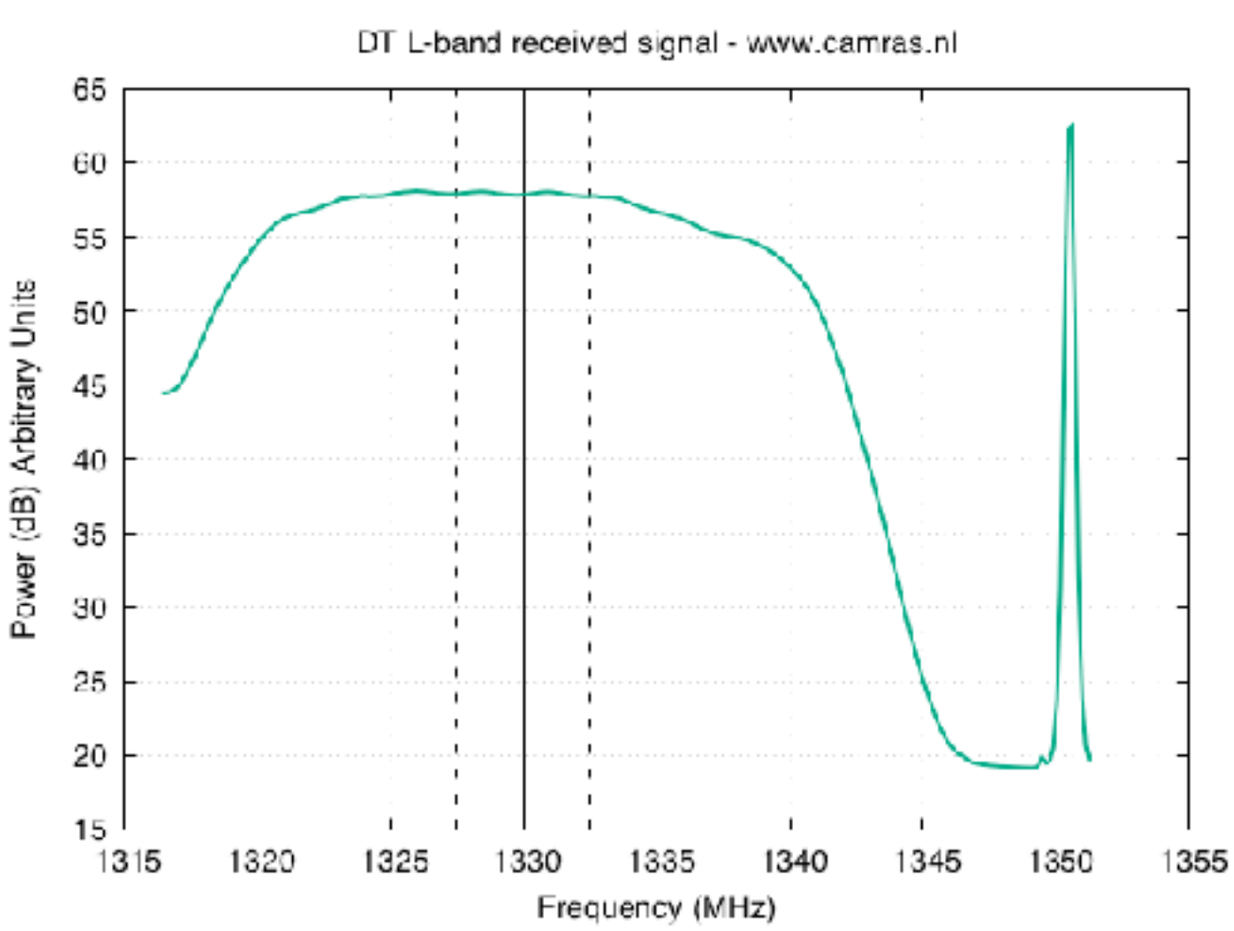
FPGA DSP Block (Xilinx DSP48)



GNU Radio Mode



- Cascaded FIR filter
  - First Filter: Large transition band
  - Second filter: steep halfband
- Implemented in FPGA
- Input: 70Ms/s real samples
- Output: 5Ms/s complex data
- GnuRadio compatible:
  - Interleaved 16 bits ints
  - Ethernet UDP Jumbo Frames
- 160Mb/s traffic



De resolutie van een Radio Telescoop

$\theta \approx 1.2\ \lambda/D$ (λ = golflengte, D = diameter)

Hubble Space Telescope:
λ = 600nm (zichtbaar licht)
D = 2.4m
θ = 0.06 boogseconde

Dwingeloo radio telescoop
λ = 6cm (5GHz)
D = 25m
θ = 600 boogseconden

Gezocht: Telescoop van 250 km?

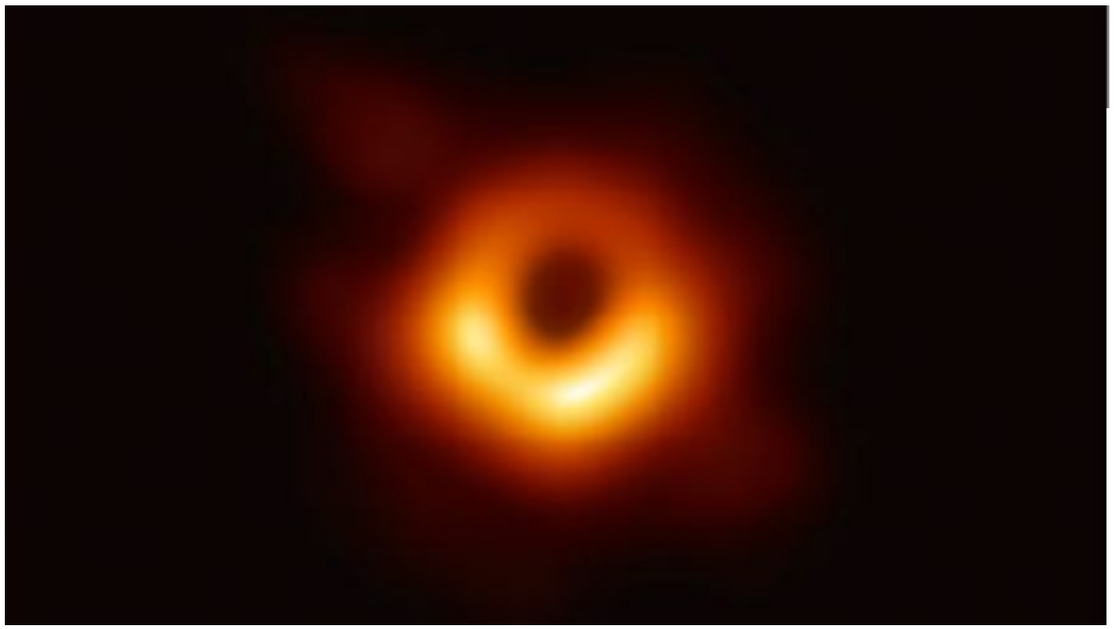
Very Long Baseline Interferometry

JIVE
Joint Institute for VLBI ERIC

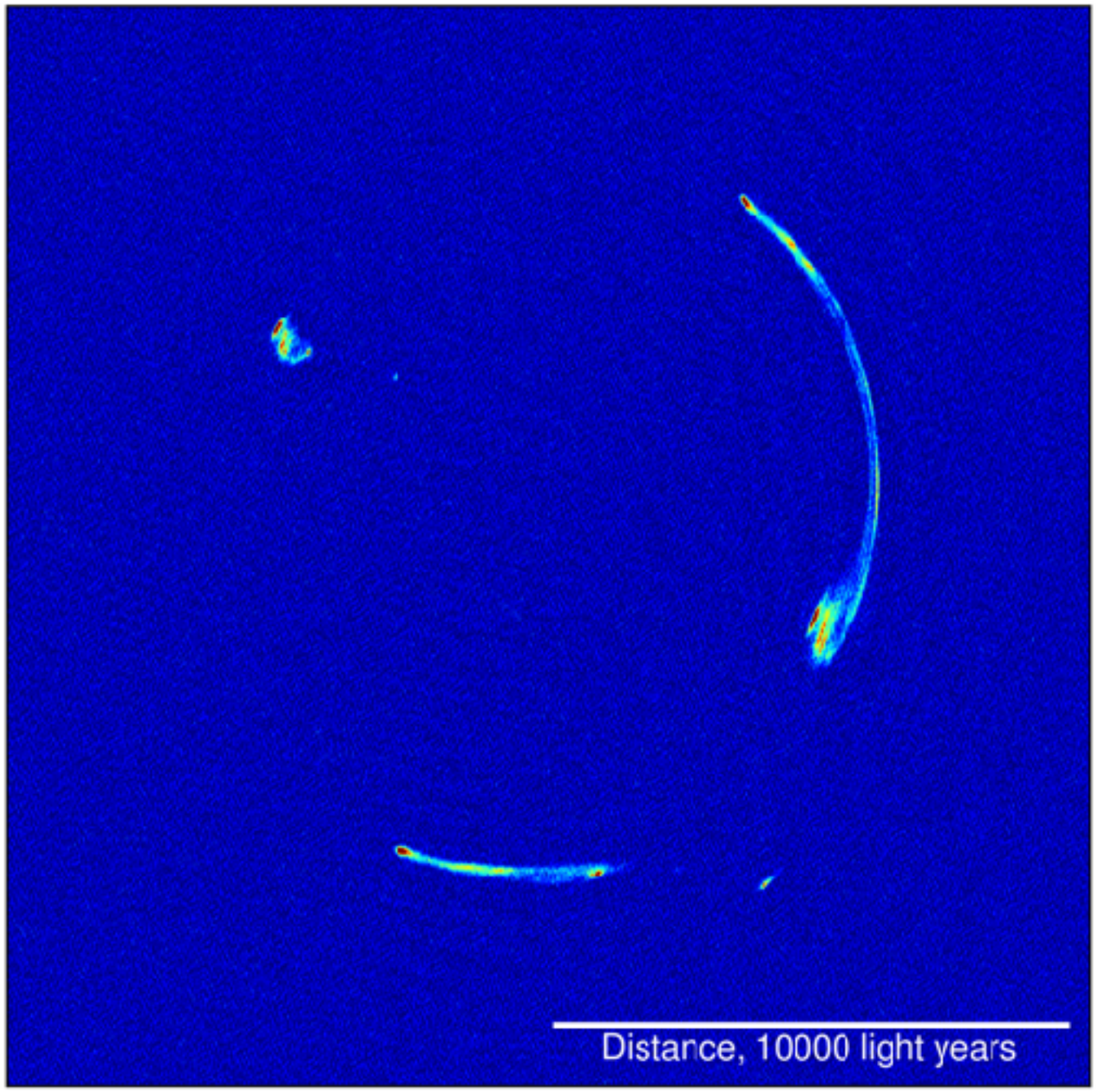
EUROPEAN vlbi NETWORK

Image by Paul Boven (boven@jive.eu). Satellite image: Blue Marble Next Generation, courtesy of Nasa Visible Earth (visibleearth.nasa.gov).

VLBI Voorbeelden



Zwart gat in M87 - EHT Consortium



Einstein Ring - C. Spingola e.a.

White Rabbit

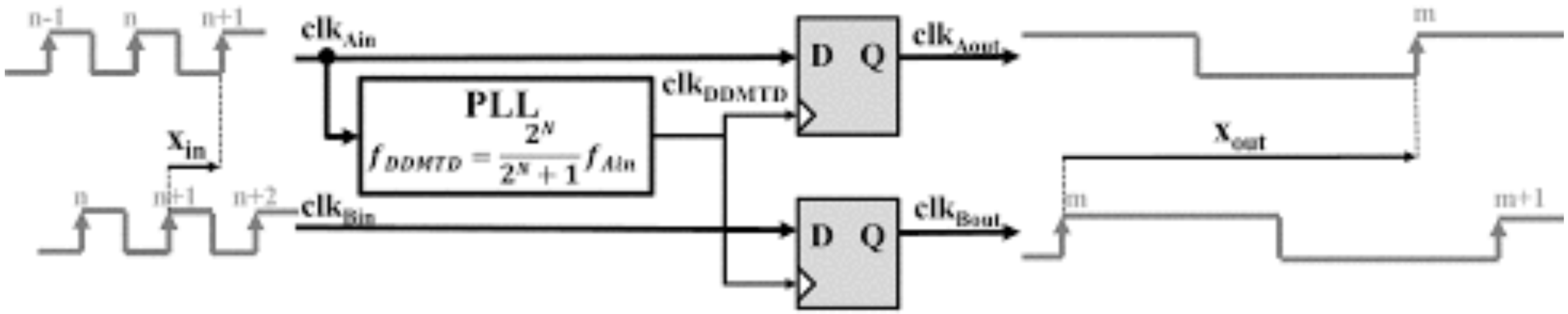
- Een open standaard voor distributie van tijd en frequentie
- 1ns over 10km, naar 1000-en eindpunten

- Origineel ontwerp door CERN, vrijgegeven als open hardware

- Glasvezel (single mode, single fiber) voor distributie
- Timing van de RTT in FPGA (ps resolutie)

- Tijd-referentie van WSRT (waterstof maser)
  - via 35km (en 169km) fiber naar DT
- Stabiliteit: ruim beter dan 10E-14 !

DDMTD



- Digital Dual Mixer Time Difference
- White Rabbit: Input is 62.5 MHz
- N=14: Helper is 62.496185 MHz
- Verschil: 3.814 kHz
- Resolutie: 1ps, 30 Hz bandbreedte

Nieuw Backend

Ettus X310

- Dual 10Gb/s SFP+
- Big FPGA
- Twee TwinRX modules
  - 10 MHz - 6GHz
  - Elk 2x 80 MHz Bandbreedte

X310

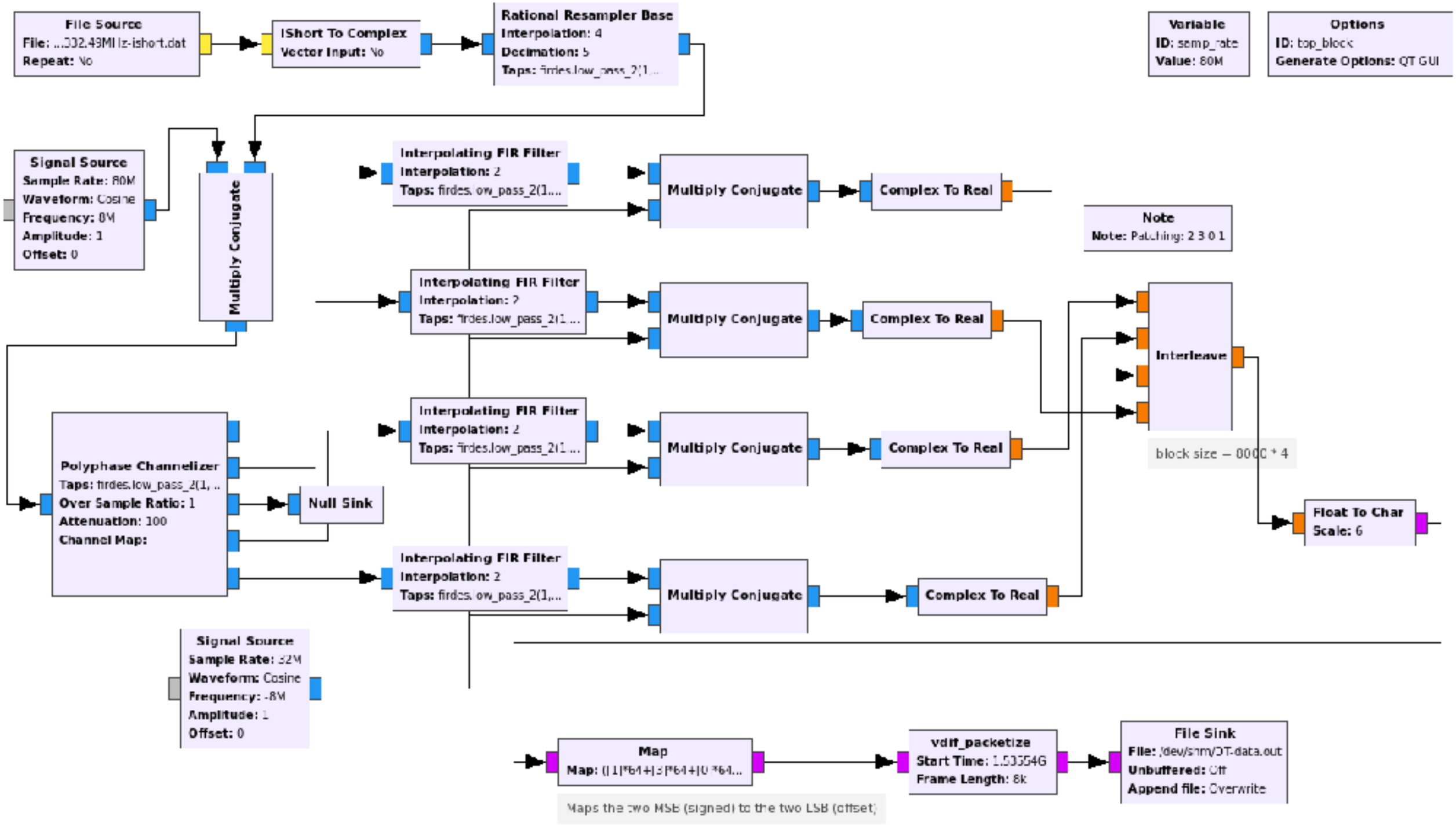
- FPGA: Xilinx Kintex7-410T
  - 406,720 cells
  - 1540 multipliers
  - >500 pins

TwinRX

Gebruik voor VLBI:

- RFNOC processing in FPGA
- H-Maser clock via White Rabbit

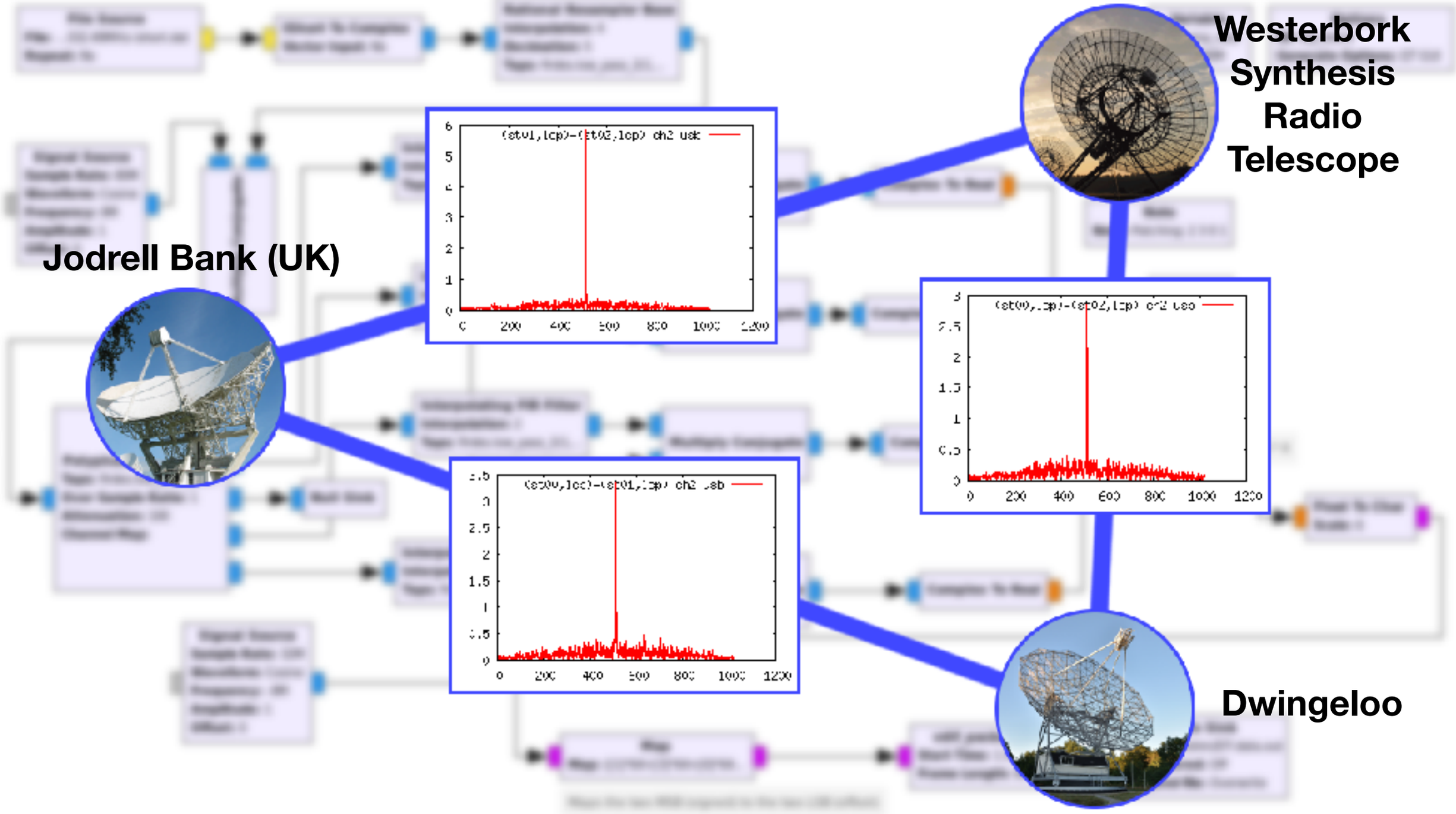
Dwingeloo VLBI



- **Runs on Ettus X310 with dual TwinRX**
- **Four of these flowcharts to get 256MHz of spectrum, 1024Mb/s data**

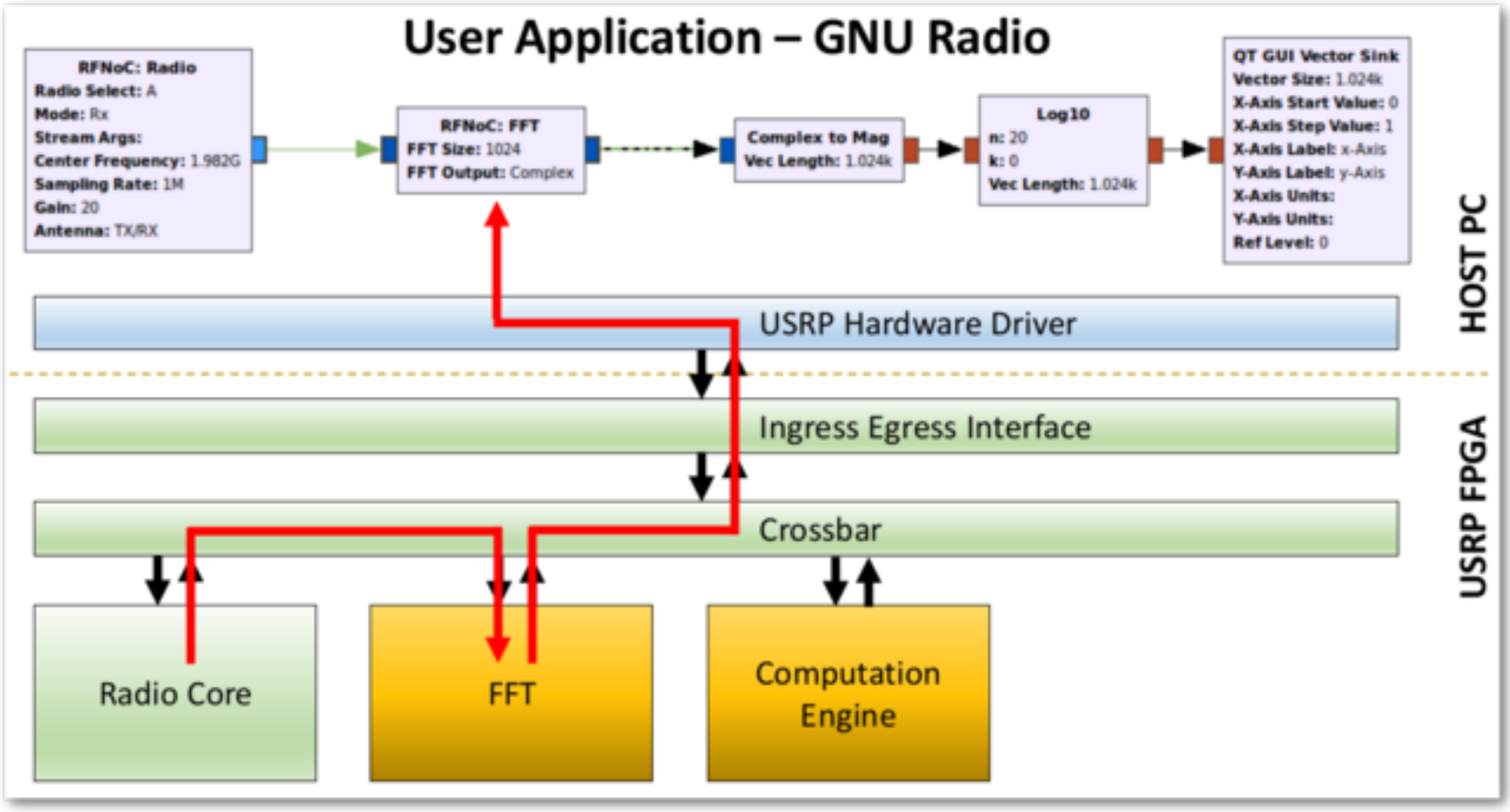
Dwingeloo VLBI fringes (again) !

2018-08-25



- Using a Rubidium (Now: White Rabbit link to H-Maser in WSRT)

RFNoC



- Deel van de signal-processing flowchart in FPGA
- Nu bezig VLBI flowchart om te zetten in Verilog
- RF-NoC: RF Network-on-Chip
- Module om eigen firmware voor USRP te schrijven

Contact Houden

- Website: http://www.camras.nl/
- Mail: info@camras.nl
- Gitlab: http://gitlab.camras.nl/public
  - Inclusief ontwerp van backend
- Twitter:
  - @Radiotelescoop (Dutch, general public)
  - @PI9CAM (English, more technical)
- Observatie data:
  - http://charon.camras.nl/public
  - Pulsars, SETI, DSLWP-B

- Nieuwe vrijwilligers zijn welkom!